

FIG. 1

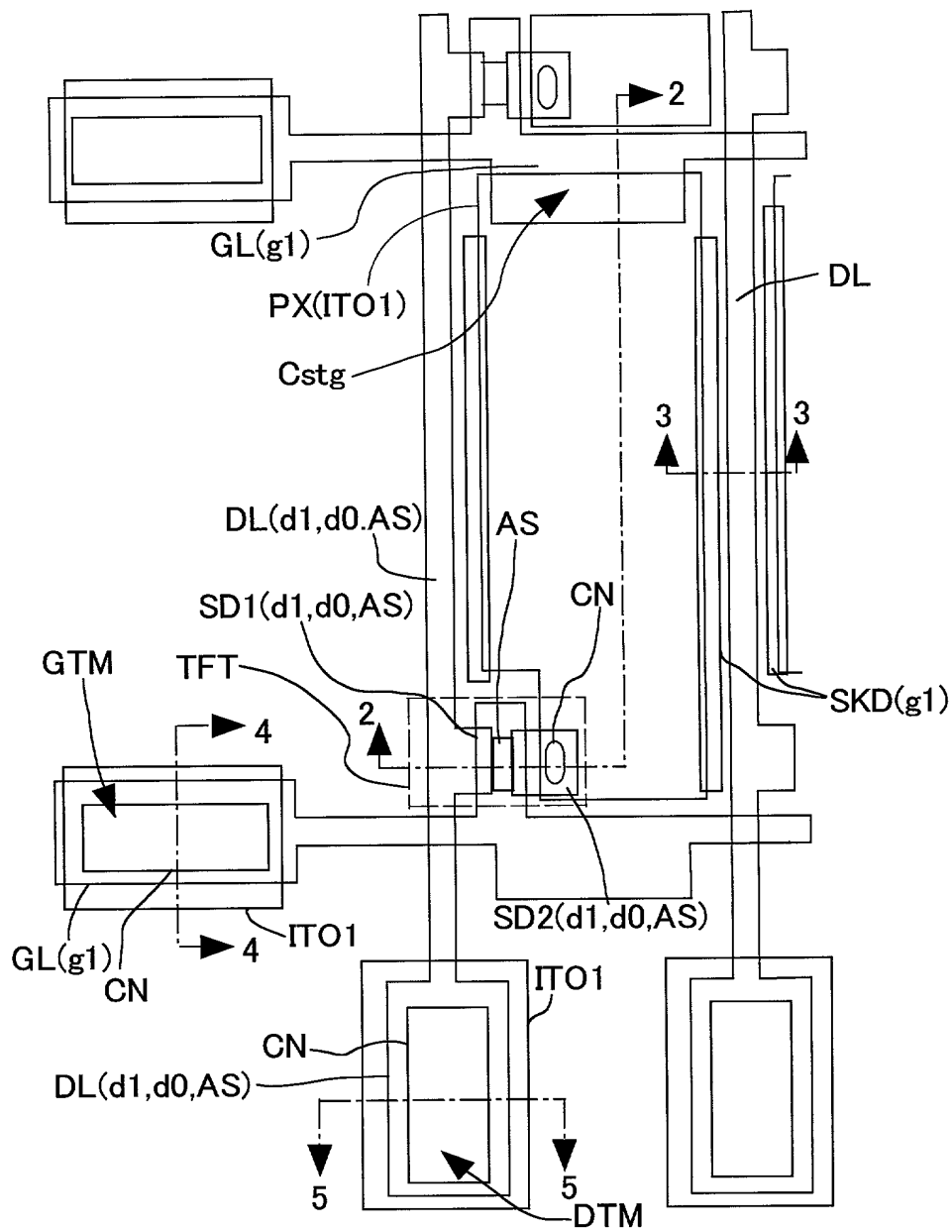


FIG. 2

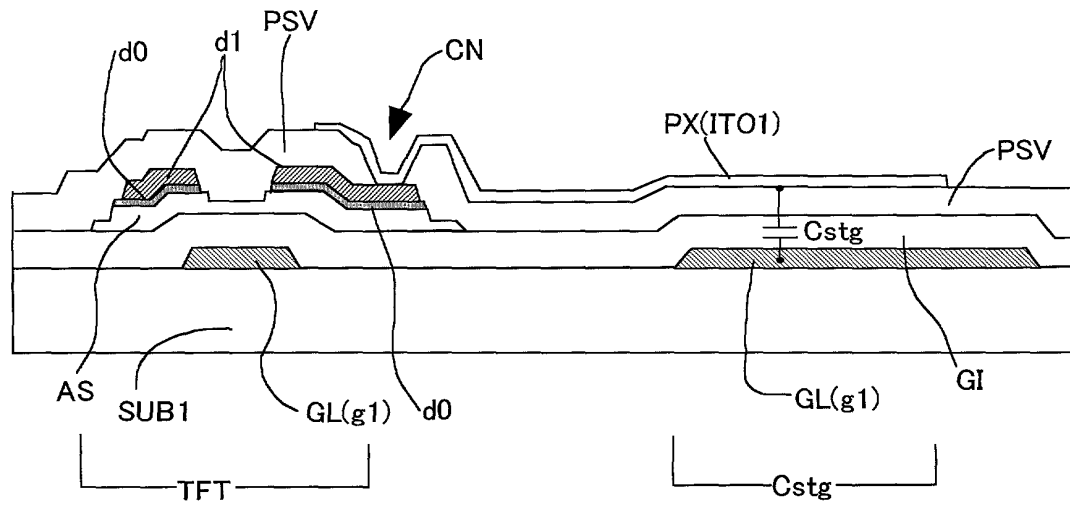


FIG. 3

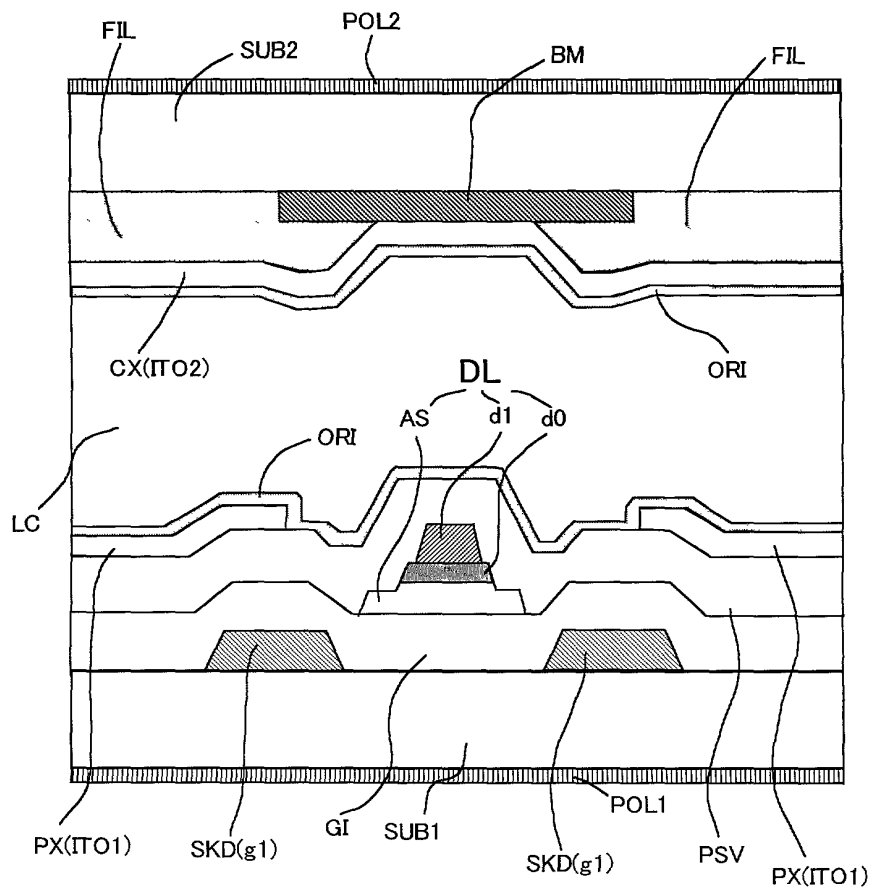


FIG. 4

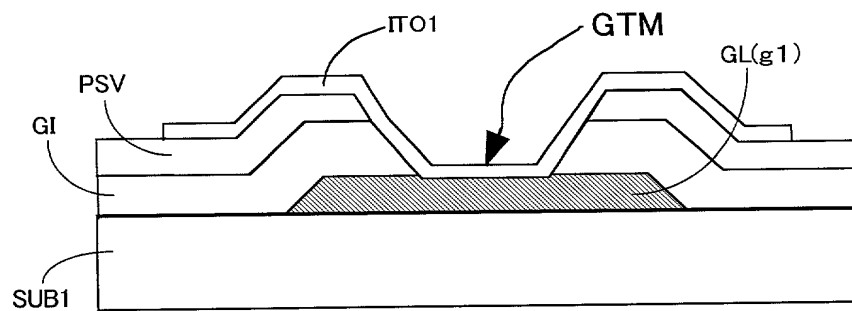


FIG. 5

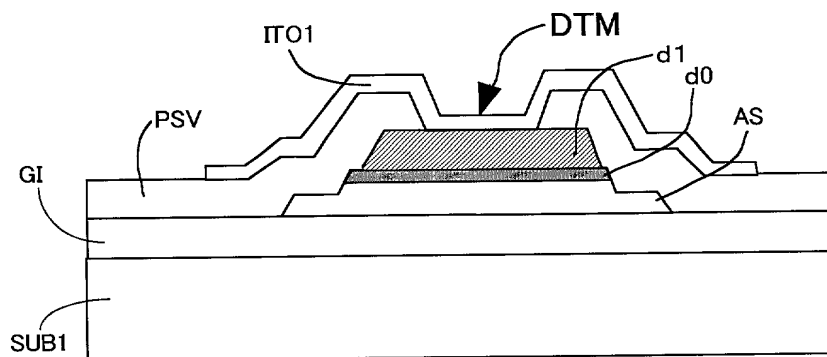


FIG. 6A

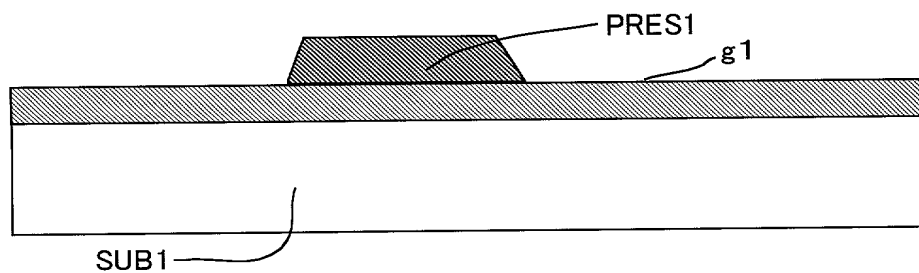


FIG. 6B

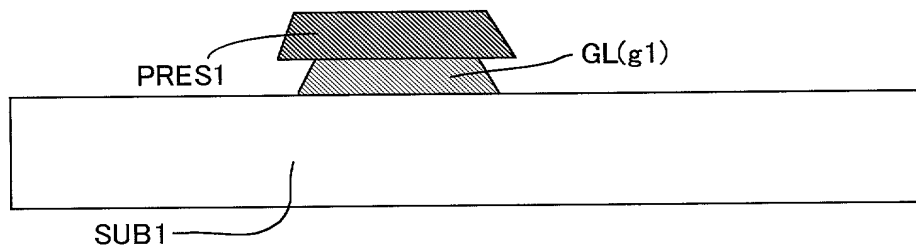


FIG. 7A

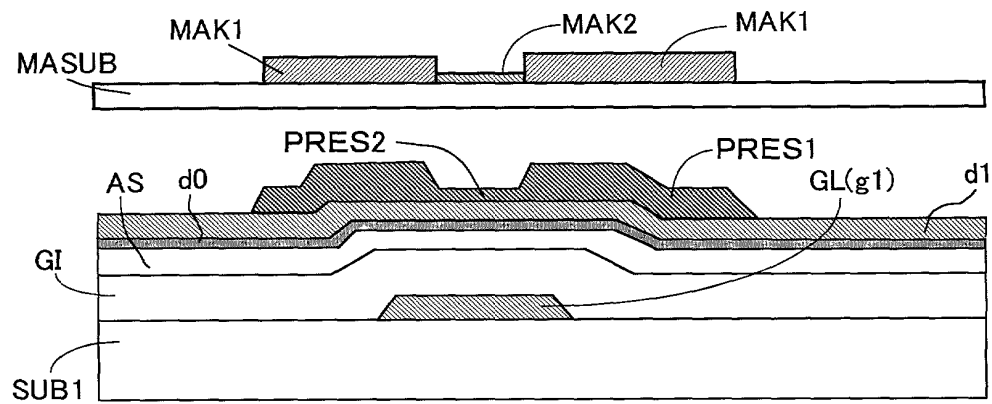


FIG. 7B

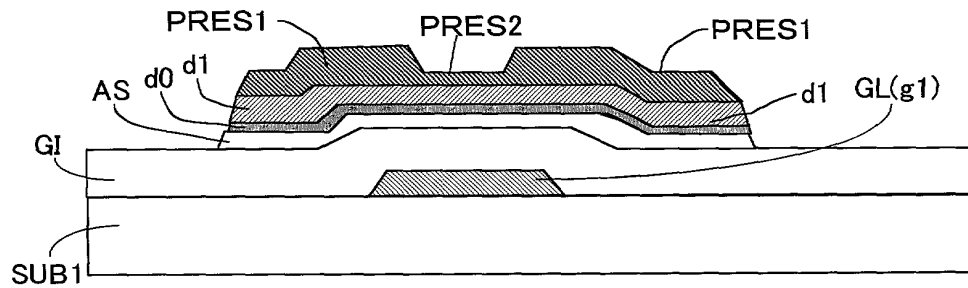


FIG. 7C

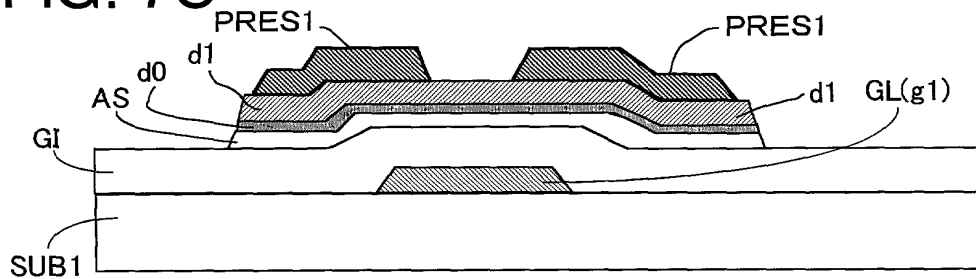


FIG. 7D

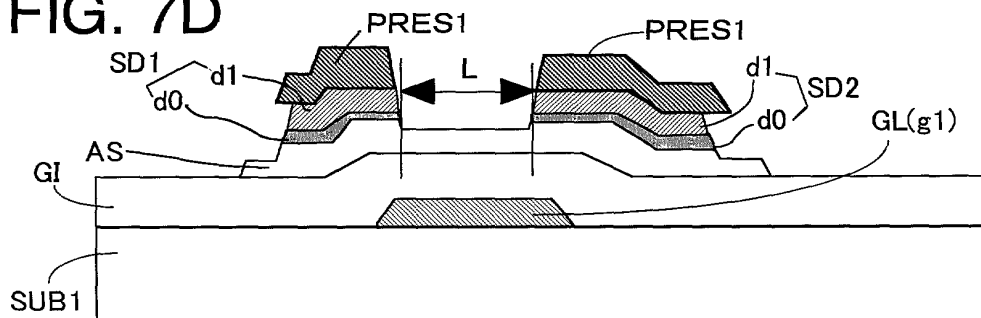


FIG. 8A

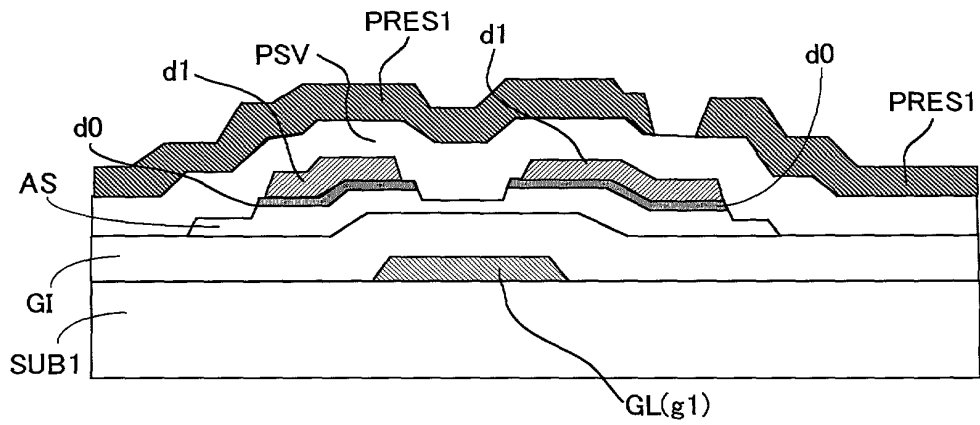
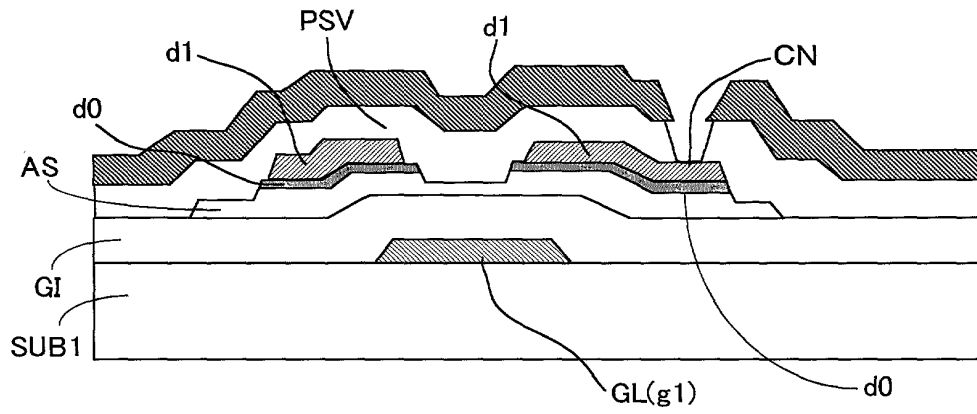


FIG. 8B



A cross-sectional view of a semiconductor device. The structure consists of several layers: a bottom substrate labeled SUB1, followed by a gate insulator layer GI, and an active layer AS. On top of the AS layer, there are two main regions: a central region with a pattern labeled PSV and a right-hand region with a pattern labeled PRES1. The PSV region contains a series of steps or terraces, with the top surface labeled d1 and the side surface labeled d0. The PRES1 region is a thick, stepped layer on the right. Below the AS layer, there is a layer labeled GL(g1) with a central rectangular pattern. At the bottom right, there is a layer labeled PX(ITO1) with a pattern labeled d0. The entire structure is shown in a perspective view, with hatching used to indicate different materials or regions.

FIG. 10

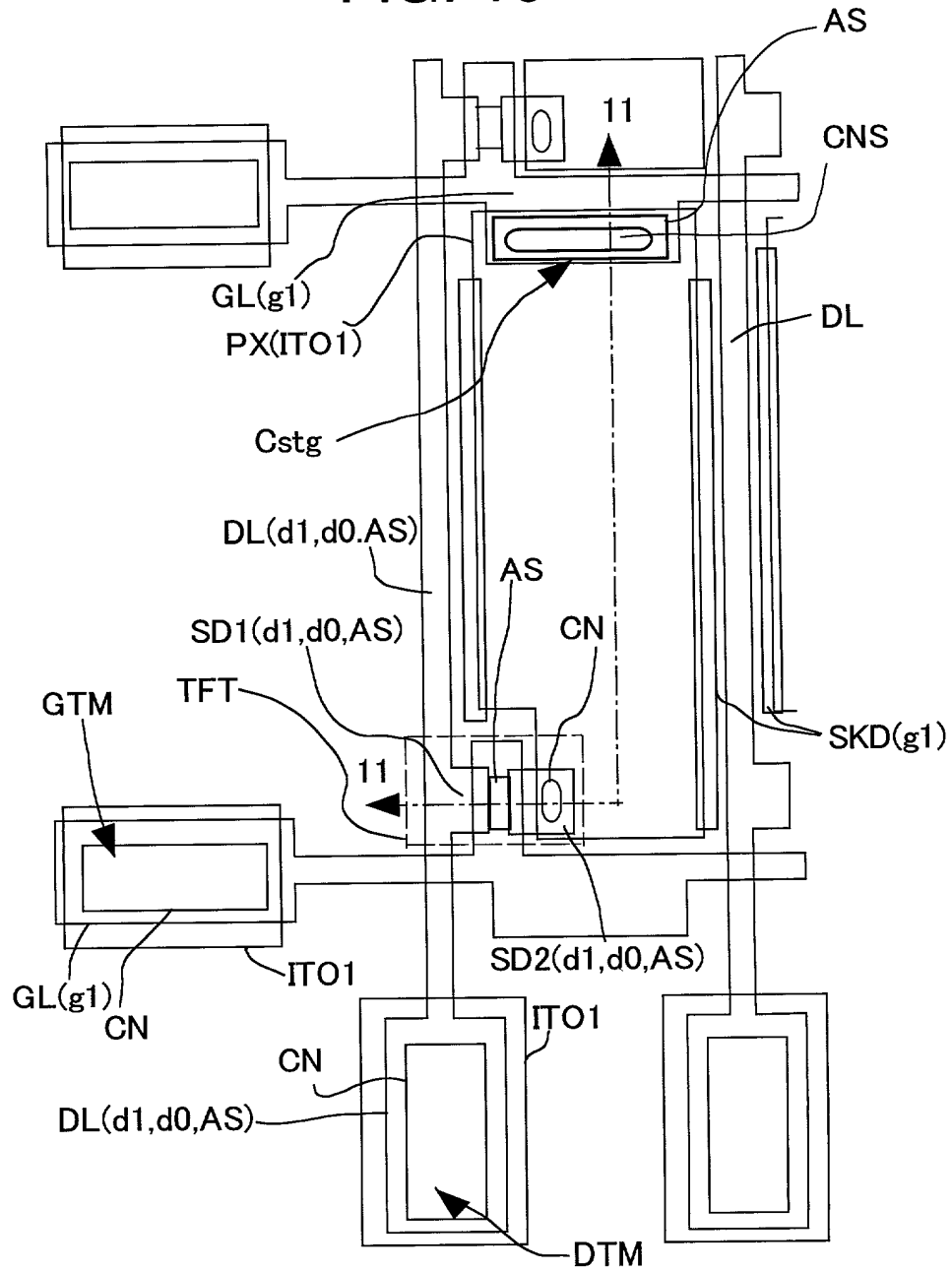


Diagram illustrating the cross-sectional structure of a semiconductor device, showing a TFT (Thin-Film Transistor) and a storage capacitor (Cstg) structure. The structure includes layers labeled: d0, d1, PSV, CN, CNS, AS, PX(ITO1), Cstg, GL(g1), GI, SD1, SD2, SUB1, and TET.

A cross-sectional view of a semiconductor device. The structure consists of a substrate (SUB1) with a gate layer (GL(g1)) and a gate insulator (GI) on top. The gate layer has a series of steps or notches. Labels include d1, d0, and AS, indicating specific dimensions or regions.

FIG. 12B

A cross-sectional view of a semiconductor device. The substrate is labeled SUB1. A gate layer (GI) is formed on the substrate, with gate spacers (GL(g1)) on either side. A patterned layer (AS) is formed on top of the gate layer, with regions labeled PRES1 and PRES2. The thickness of the gate layer is indicated as d0 and the thickness of the gate spacers as d1.

FIG. 13A

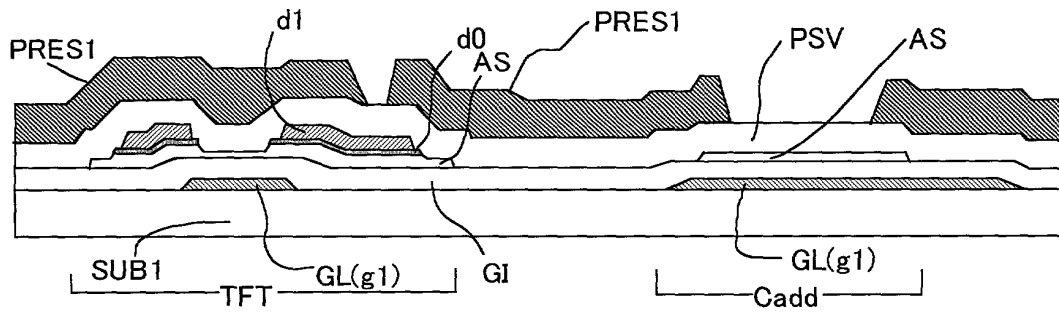


FIG. 13B

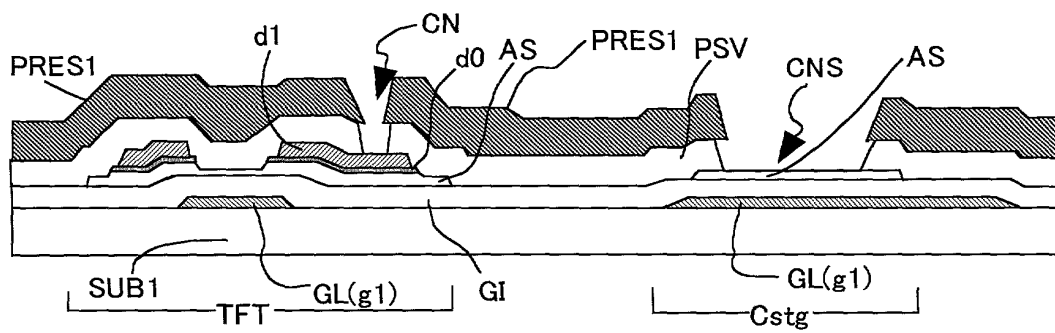


FIG. 14

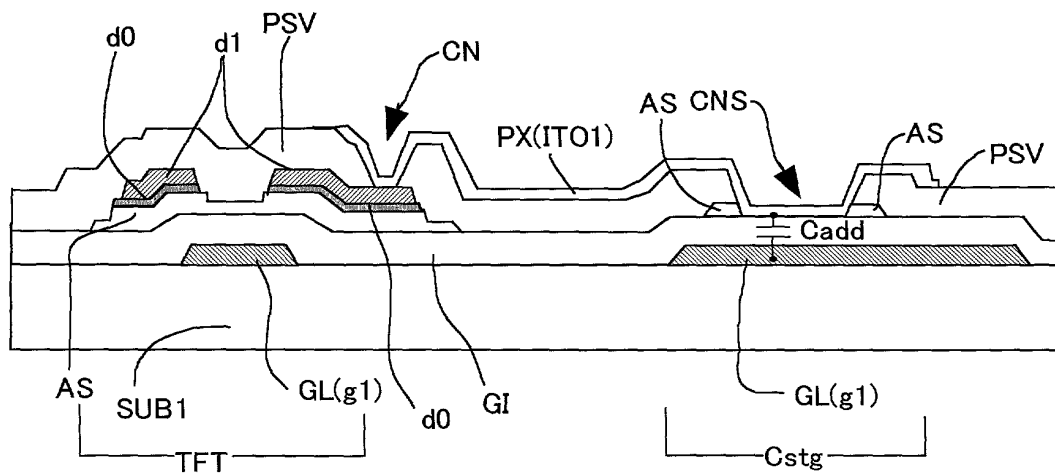


FIG. 15A

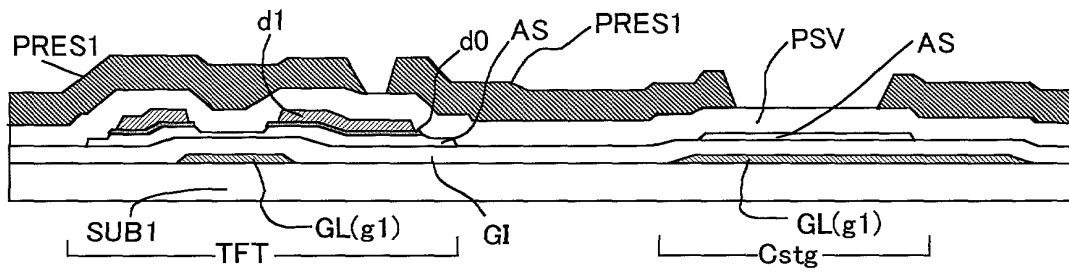


FIG. 15B

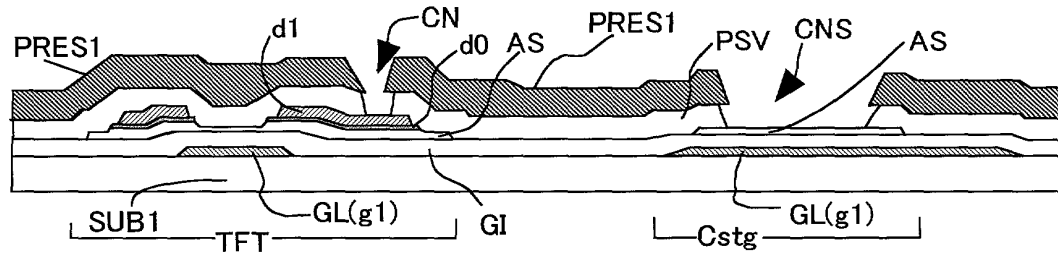


FIG. 15C

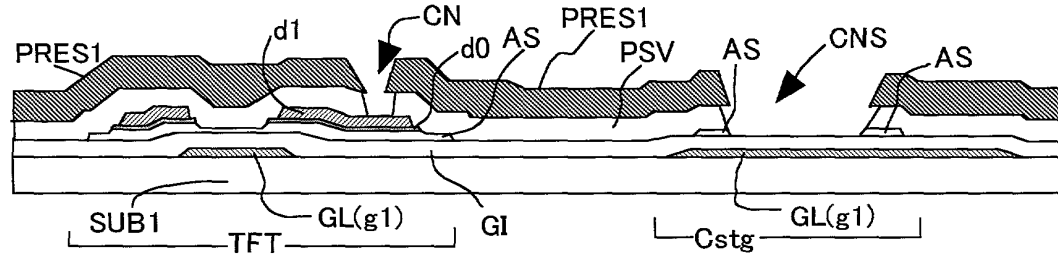
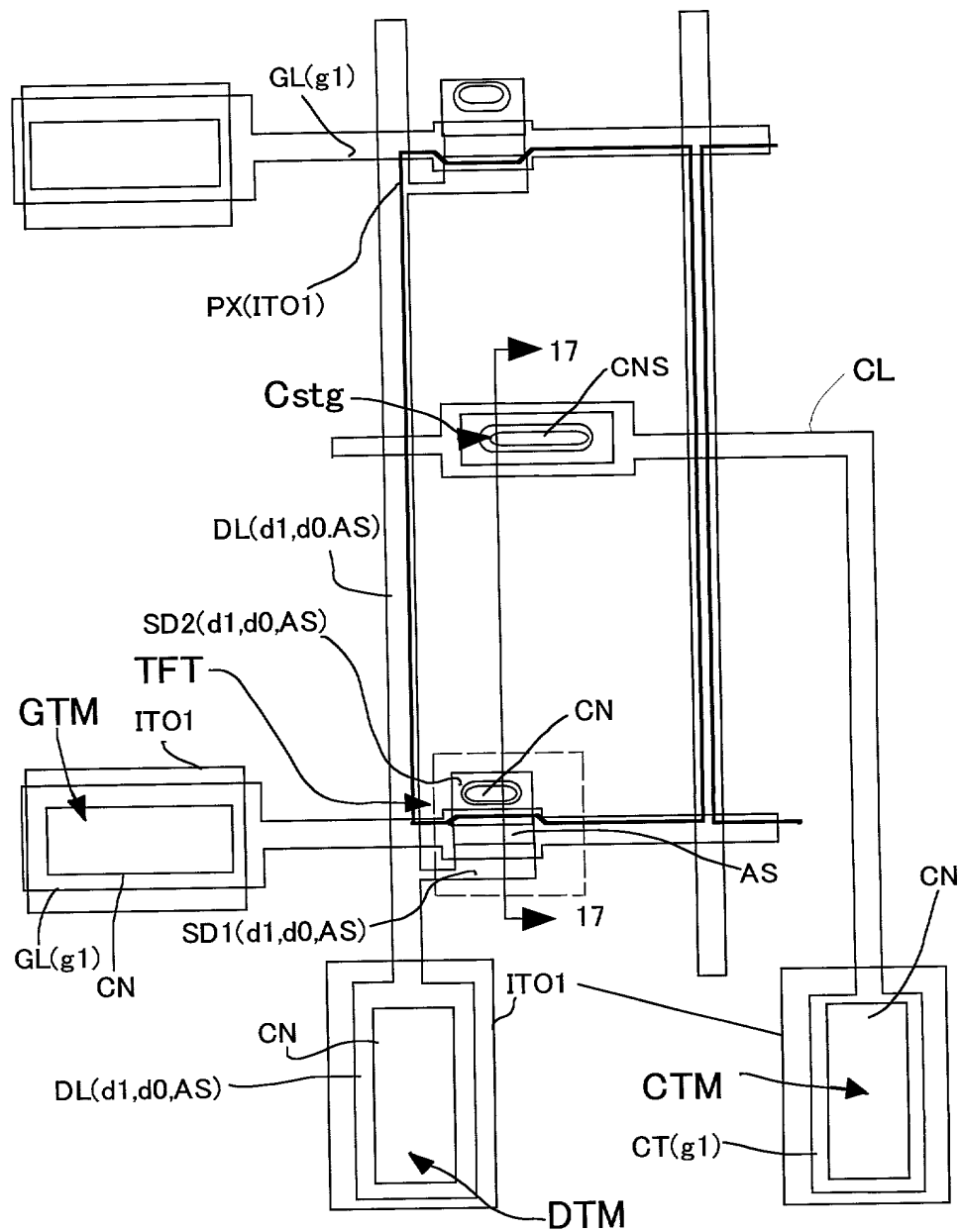


FIG. 16



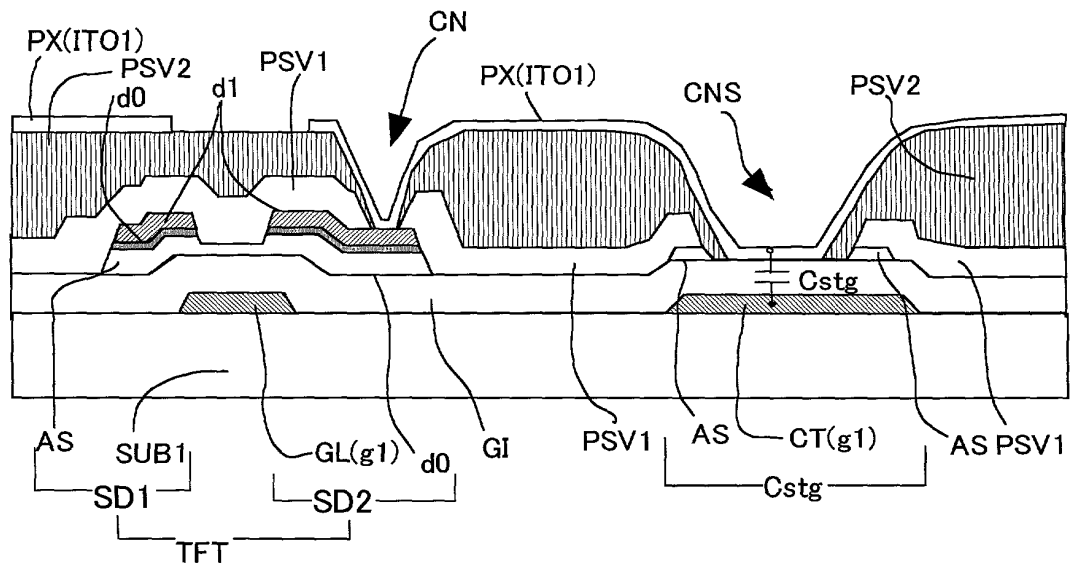
[illegible]

FIG. 18A

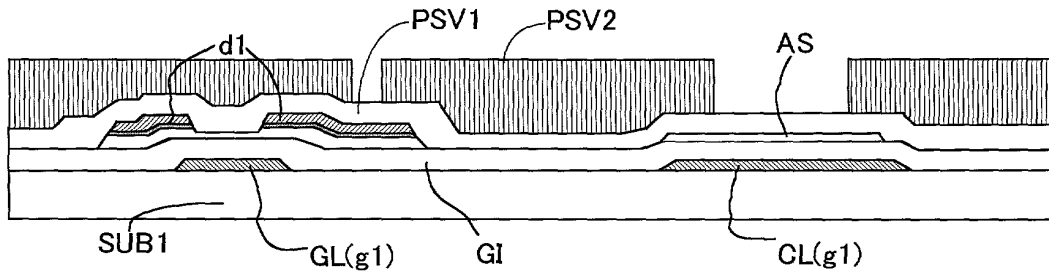


FIG. 18B

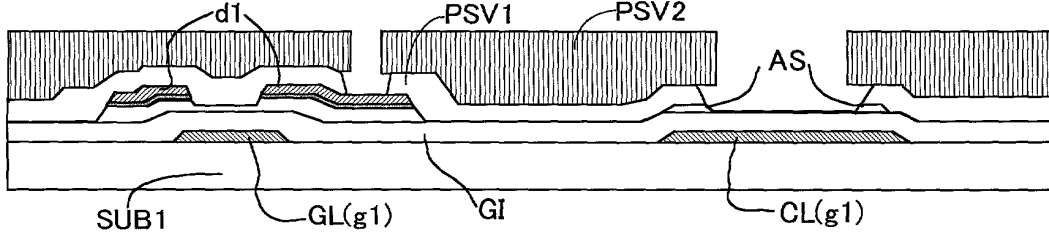


FIG. 18C

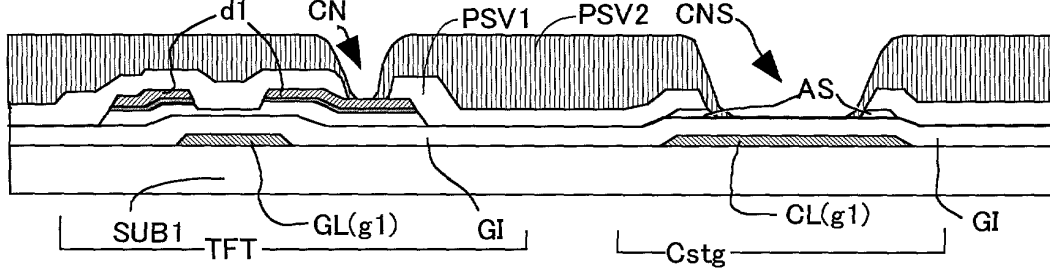


FIG. 19

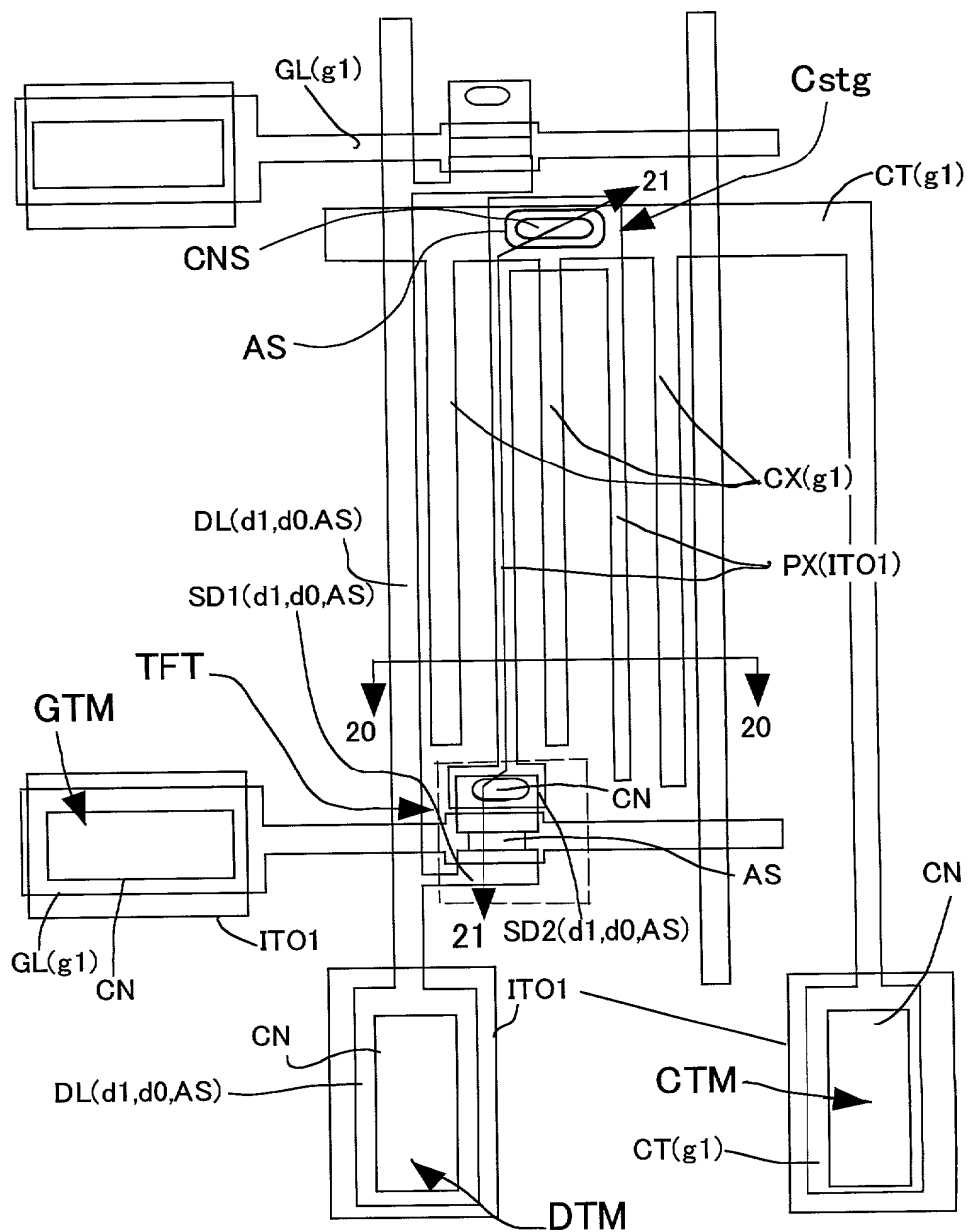


FIG. 20

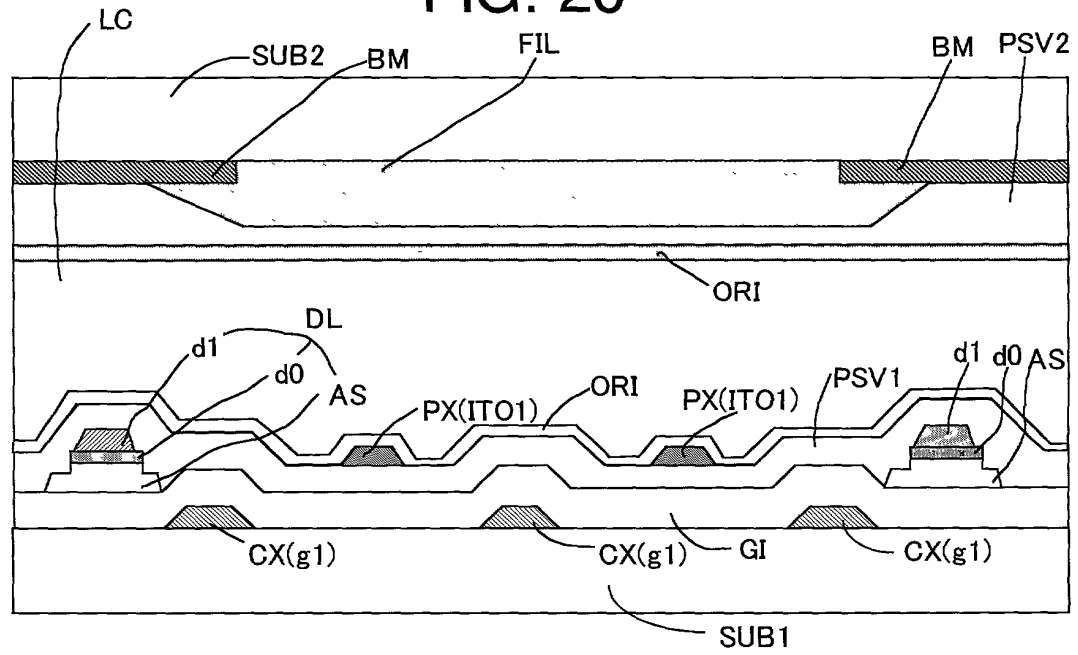


FIG. 21

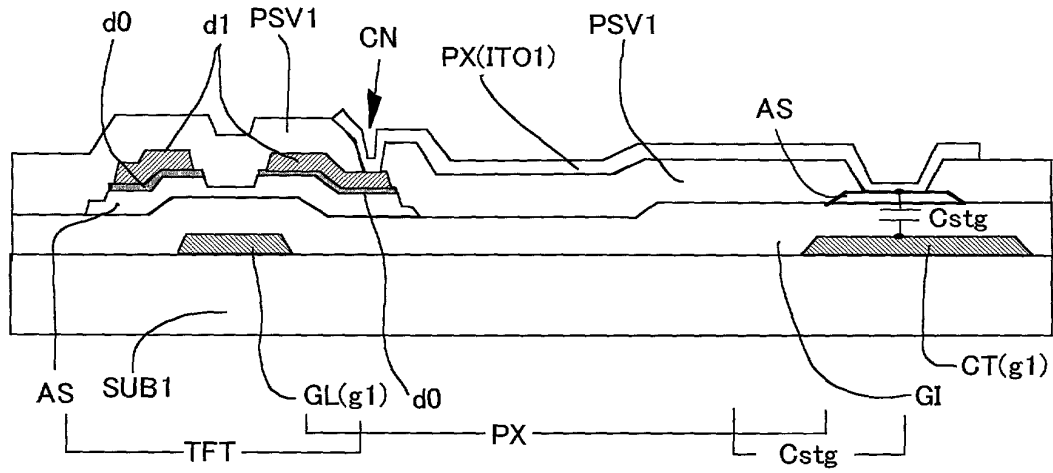


FIG. 22

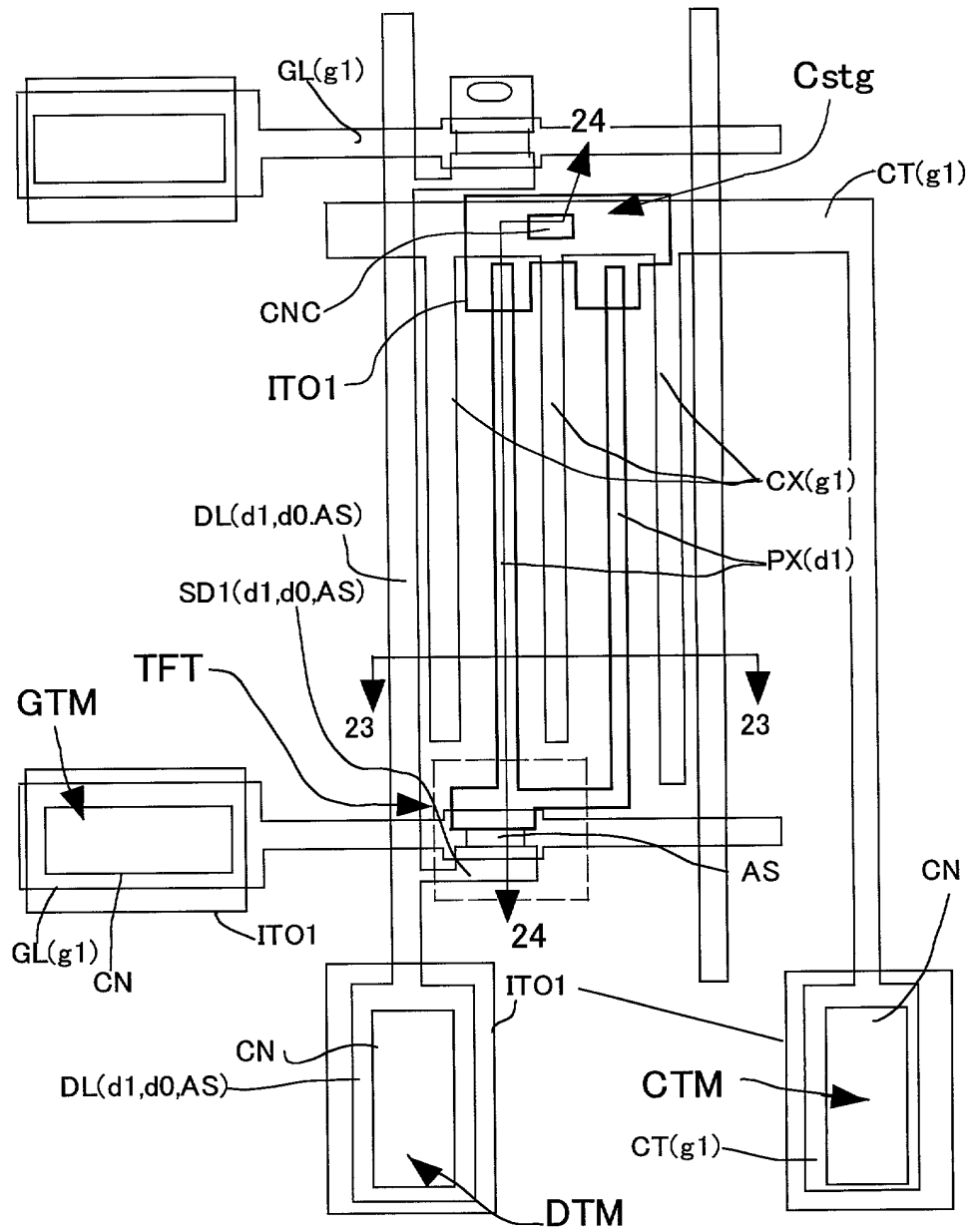


FIG. 23

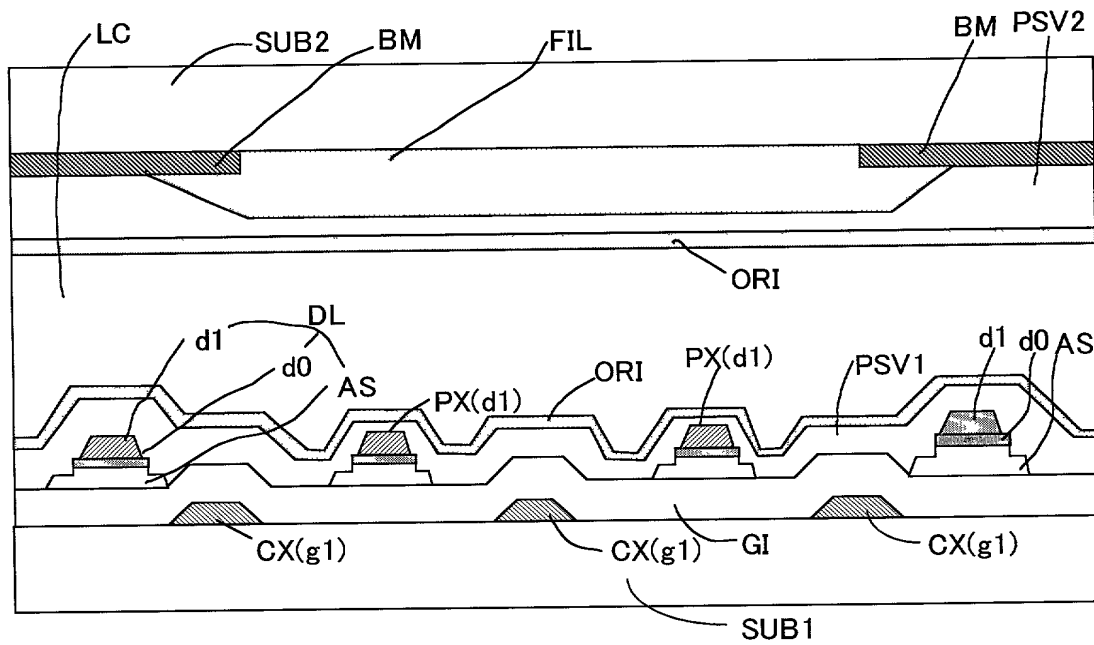


FIG. 24

